

Appl. No. 10/761,702
Examiner: Warren, Matthew E, Art Unit 2815
In response to the Office Action dated October 19, 2005

Date: April 14, 2006
Attorney Docket No. 10113671

REMARKS

Responsive to the Office Action mailed on October 19, 2005 and the Advisory Action mailed February 10, 2006 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1, 3-9, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over APAF in view of Maex et al (U.S. 6,323,555, hereinafter "Maex"). Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over APAF in view of Maex and Hedrick et al (US 2004/0207084 A1).

In this paper, claim 1 is amended as described in further detail below. New dependent claim 28 is added. Support for the amendments and new claim can be found at least on page 7 of the application and Figs. 6A-6C. Claim 27 is amended to correspond to the amendment to claim 1. Claims 8 and 25-26 are canceled. Thus, on entry of this amendment, claims 1, 3-7, 9 and 27-28 remain in the application.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Rejections Under 35 U.S.C. 103(a)

Claims 1, 3-9, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over APAF in view of Maex. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over APAF in view of Maex and Hedrick. To the extent that the grounds of the rejections may be applied to the claims now pending in this application, they are respectfully traversed.

As amended, claim 1 recites a bit line contact structure of a memory device, comprising:

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a substrate having a transistor of the memory device thereon, the transistor having a raised gate electrode, a drain region, and a source region;

a composite dielectric layer, sequentially having a first dielectric layer, barrier layer, and second dielectric layer, directly on the transistor, the first dielectric layer comprising polyimide, the composite dielectric layer having an opening exposing the drain region; and

a tungsten layer or a polysilicon layer in the opening,

wherein the thickness of the first dielectric layer is thicker than the second dielectric layer.

Whether taken alone or in combination, the cited references fail to teach or suggest the limitation of a tungsten layer or a polysilicon layer in the opening, as recited in amended claim 1.

MPEP 2142 reads in part:

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on to state:

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered

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in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

APAF only teaches a conductive layer in the opening. Maex on the other hand teaches that the conductive pattern is composed of a metal selected from a group comprising Al, Cu, Al-alloy or Cu-alloy. See col. 3, lines 27-35 of Maex. Neither reference teaches or suggests the claim feature of a tungsten layer or a polysilicon layer in the opening.

Whether taken alone or in combination, the cited references fail to teach or suggest the thickness of the first dielectric layer is thicker than the second dielectric layer, as recited in amended claim 1.

The structure of APAF comprises raised transistors. A dielectric layer fills the openings between adjacent transistors. With reference to Fig. 1H of Maex, it is evident that the first dielectric layer 2 and the second dielectric layer 5 have substantially the same thickness. It follows that if the composite dielectric layer of Maex were combined with the structure of APAF, the first dielectric layer and the second dielectric layer would have substantially the same thickness.

By contrast, claim 1 recites that the first dielectric layer is thicker than the second dielectric layer. One advantage of the claimed arrangement is that the barrier layer is in a relatively higher position. This helps avert crossing of the barrier layer and the transistors. Another advantage is the better self-alignment when the first dielectric layer is thicker than the second dielectric layer. The combination proposed by the Examiner does not achieve these advantages.

It is therefore Applicant's belief that even when taken in combination, the prior art references relied upon by the Examiner do not teach or suggest all the limitations of claim 1. For at least this reason, a *prima facie* case of obviousness cannot be established in connection with this claim. Furthermore, as it is Applicant's belief that a *prima facie* case of obviousness is not established for claim 1, the Examiner's arguments in regard to the dependent claims are

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considered moot and are not addressed here. Allowance of claims 1, 3-7, 9 and 27-28 is respectfully requested.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



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